su3_bench, a Micro-benchmark for Exploring Exascale Era Programming Models, Compilers and Runtimes

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The su3_bench benchmark

- su3_bench was developed to provide a means to explore different programming methodologies using a simple, but nontrivial, mathematical kernel

- Derived from the MILC Lattice QCD (LQCD) code
  - Matrix-matrix and matrix-vector SU(3) (special unitary group of degree 3) operations are a fundamental building block of LQCD applications
  - Most LQCD applications use domain specific implementations (libraries) written in machine specific languages and/or intrinsics ...
  - Hence performance portable methodologies are of interest

- Kernel calculates an SU(3) matrix-matrix multiply of complex numbers
  - Benchmark operates over a lattice of dimension = $L^4$

- [https://gitlab.com/NERSC/nersc-proxies/su3_bench](https://gitlab.com/NERSC/nersc-proxies/su3_bench)
  - Released as open-source software under LBNL’s modified BSD license
su3_bench data structures

• SU(3) matrix definition (72 bytes single, 144 bytes double)

```c
typedef struct { std::complex<float> e[3][3]; } fsu3_matrix;
typedef struct { std::complex<double> e[3][3]; } dsu3_matrix;
#if (PRECISION==1)
  #define su3_matrix    fsu3_matrix
#else
  #define su3_matrix    dsu3_matrix
#endif
```

• Site definition
  • Based on MILC’s lattice.h, but reduced to bare minimum of fields

```c
typedef struct {
  su3_matrix link[4];  // the fundamental gauge field
  int x,y,z,t;         // coordinates of this site
  int index;           // my index in the array
  char parity;         // is it even or odd?
#if (PRECISION==1)
  int pad[2];          // pad out to 64 byte alignment
#else
  int pad[10];
#endif
} site __attribute__ ((aligned));
```

su3_bench performs a 3x3 complex matrix-matrix multiply for each gauge field in the 4 lattice dimensions.

\[ C = A \times B \]
The kernel: $C = A \times B$

for (i=0; i<total_sites; ++i)  // L^4 lattice sites
    for (j=0; j<4; ++j)  // 4 links, SU(3) matrices, per site
        for (k=0; k<3; k++)  // 3x3 matrix elements per link
            for (l=0; l<3; l++) {
                cc = {0.0, 0.0, 0.0};
                for (m=0; m<3; m++)  // 3x1 dot product per matrix element
                    cc += A[i].link[j].e[k][m] * B[j].e[m][l];
                C[i].link[j].e[k][l] = cc;
            }

Nominal GPU parallelization strategy:
• For each site, create $4 \times 3 \times 3 = 36$ threads
• Each thread does a single $3 \times 1$ vector dot product
• Reduces the number of Sites/group and alleviates cache pressure
Analytical roofline model

- A & C are lattices of size $L^4$ sites
  - $su3\_matrix[4] \rightarrow 288$ bytes/site
  - A is read once per iteration
  - C is written once per iteration
- B is a single $su3\_matrix[4]$ array
  - Relatively small, should stay in cache
- Total Bytes = 576 Bytes (single-precision)
- Total FLOPS = 864 FLOPS/site
- Arithmetic Intensity (FLOPs/Byte)
  - $AI = \frac{864}{576} = 1.5$ single-precision
  - $AI = 0.75$ double-precision

Su3_bench: Cori GPU Analytical Roofline

- $14,274$ GF/s (SGEMM)
- $846$ GB/sec (BabelStream)
- Performance $\leq 1,269$ GFLOPS/sec
## Test beds used for this study

<table>
<thead>
<tr>
<th></th>
<th>NERSC: Cori GPU</th>
<th>OLCF: Lyra</th>
<th>ALCF: Iris</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPU architecture</td>
<td>Nvidia V100</td>
<td>AMD MI-60</td>
<td>Intel Gen9 NEO</td>
</tr>
<tr>
<td># units/device</td>
<td>80 SM</td>
<td>64 CU</td>
<td>72 EU</td>
</tr>
<tr>
<td>FP32 cores/simd lanes</td>
<td>5120 = SMs*64</td>
<td>4096 = CUs*64</td>
<td>576 = EUs<em>2</em>4</td>
</tr>
<tr>
<td>FP64 cores/simd lanes</td>
<td>2560 = SMs*32</td>
<td>same</td>
<td>144 = EUs<em>1</em>2</td>
</tr>
<tr>
<td>L2 cache</td>
<td>6144 KB</td>
<td>4096 KB</td>
<td>1536 KB</td>
</tr>
<tr>
<td>L1 cache</td>
<td>6400 KB/SM (shared)</td>
<td>16 KB/CU</td>
<td></td>
</tr>
<tr>
<td>TFLOP/s peak</td>
<td>13.4/15.7 single 6.72/7.83 double</td>
<td>9.83/14.8 single 4.92/7.37 double</td>
<td>1.32 single 0.331 double</td>
</tr>
<tr>
<td>TFLOP/s sustained</td>
<td>14.3(1) single 7.05(1) double</td>
<td>11.2(1) single 5.63(1) double</td>
<td>1.21(3) single 0.302(3) double</td>
</tr>
<tr>
<td>Gbyte/s</td>
<td>897(2) peak 847(2) sustained (94%)</td>
<td>1024(2) peak 816(2) sustained (80%)</td>
<td>25.6(3)</td>
</tr>
</tbody>
</table>

1. Using mt-dgemm benchmark
2. Using BabelStream benchmark
3. Using Empirical Roofline Toolkit, single-precision is derived from double-precision
## Cori-GPU Programming Environments

<table>
<thead>
<tr>
<th>CUDA</th>
<th>HIP</th>
<th>OpenCL</th>
<th>OpenMP</th>
<th>OpenACC</th>
<th>SYCL</th>
<th>Intel DPCPP</th>
</tr>
</thead>
<tbody>
<tr>
<td>CUDA 10.2.89</td>
<td>rocm-3.3.0</td>
<td>Version 1.2</td>
<td>llvm/10.0.0</td>
<td>PGI/19.10</td>
<td>Codeplay ComputeCpp 1.3.0</td>
<td>sycl branch</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GCC</td>
<td>CUDA 10.1.243</td>
<td>Cori GPU module</td>
<td>With POCL</td>
<td>• With Codeplay developed</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OpenCL in CUDA driver</td>
<td>PGI/19.20-alpha2</td>
<td>Cray PE</td>
<td>(see OpenCL)</td>
<td>NVPTX backend</td>
</tr>
<tr>
<td></td>
<td></td>
<td>POCL: based on llvm 9 w/SPIRV-LLVM</td>
<td>CUDA 9.2.148</td>
<td></td>
<td>Experimental PTX target</td>
<td>• CUDA 10.1.243</td>
</tr>
<tr>
<td></td>
<td></td>
<td>translator; CUDA 9.2.148</td>
<td></td>
<td></td>
<td>hipSYCL</td>
<td></td>
</tr>
</tbody>
</table>

- Environments in bold where used for this study
- Environments in grey are available, but not explored here
  - I will note that POCL outperformed Nvidia’s OpenCL driver by 22% on average
Early Results (Fall 2019)

<table>
<thead>
<tr>
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<th>OpenACC</th>
<th>OpenCL</th>
<th>SYCL</th>
</tr>
</thead>
<tbody>
<tr>
<td># threads/SM</td>
<td>128</td>
<td>36</td>
<td>N/A</td>
<td>128</td>
<td>128</td>
</tr>
<tr>
<td>GFLOPS/sec</td>
<td>1112</td>
<td>104</td>
<td>810</td>
<td>1095</td>
<td>5.8</td>
</tr>
<tr>
<td>analytical roofline</td>
<td>1269</td>
<td>1269</td>
<td>1269</td>
<td>1269</td>
<td>1269</td>
</tr>
</tbody>
</table>

- Note: Log scale!
- CUDA and OpenCL perform near roofline
- OpenACC is respectable
- OpenMP & SYCL have serious issues
OpenMP Workaround

Nominal Implementation: one thread/dot product

```c
#pragma omp target teams distribute \
    thread_limit(threads_per_team)
for(int i=0; i<total_sites; ++i) {
    #pragma omp parallel for collapse(3)
    for (int j=0; j<4; ++j) {
        for(int k=0;k<3;k++) {
            for(int l=0;l<3;l++) {
                Complx cc = {0.0, 0.0};
                for(int m=0;m<3;m++)
                    cc += d_a[i].link[j].e[k][m] * d_b[j].e[m][l];
                d_c[i].link[j].e[k][l] = cc;
            }
        }
    }
}
```

Workaround: OpenCL like implementation\(^2\), w/manual collapse

```c
size_t num_work_items = total_sites * threads_per_team;
#pragma omp target teams distribute parallel for
for (int id =0; id < num_work_items; id++) {
    int i = id/36;
    int j = (id%36)/9;
    int k = (id%9)/3;
    int l = id%3;
    Complx cc = {0.0, 0.0};
    for(int m=0;m<3;m++)
        cc += d_a[i].link[j].e[k][m] * d_b[j].e[m][l];
    d_c[i].link[j].e[k][l] = cc;
}
```

\( \rightarrow \) LLVM implementation: end of parallel region forces a flush after each iteration, resulting in excessive memory traffic\(^1\)

1. Thanks to Chris Daley (LBL) for help with implementation and identifying the flush “feature”
2. Thanks to Xinmin Tian (Intel) for workaround and Intel compiler optimizations
SYCL Workaround

Nominal Implementation: array indexing

```cpp
auto d_a = a_buf.get_access<cl::sycl::access::mode::read>(cgh);
auto d_b = b_buf.get_access<cl::sycl::access::mode::read>(cgh);
auto d_c = c_buf.get_access<cl::sycl::access::mode::discard_write>(cgh);

cgh.parallel_for<class k_mat_nn>(cl::sycl::nd_range<1>{total_wi, wgsize}, [=](cl::sycl::nd_item<1> item) {
    size_t myThread = item.get_global_id(0);
    size_t mySite = myThread/36;
    if (mySite < total_sites) {
        int j = (myThread%36)/9;
        int k = (myThread%9)/3;
        int l = myThread%3;
        Complx cc = {0.0, 0.0};
        for (int m=0;m<3;m++) {
            const auto aa = d_a[mySite].link[j].e[k][m];
            const auto bb = d_b[j].e[m][l];
            cc += aa * bb;
        }
        d_c[mySite].link[j].e[k][l] = cc;
    }
});
```

SYCL 1.2.1 spec bug:
For dataT operator[] using read only mode:
“Returns the value of the element stored within the SYCL buffer this SYCL accessor is accessing at the index specified by index.”

Workaround: Pointer indexing

```cpp
for (int m=0;m<3;m++) {
    const auto aa = (d_a.get_pointer() + mySite)->link[j].e[k][m];
    const auto bb = (d_b.get_pointer() + j)->e[m][l];
    cc += aa * bb;
}
d_c[mySite].link[j].e[k][l] = cc;
```

= 5.8 GF/s

= 816 GF/s !!!

1. Thanks to Thomas Applencourt (ANL) for figuring out pointer reference performs well
2. Thanks to John Pennycook (Intel) for figuring out SYCL spec issue
Results after workarounds

- CUDA, OpenCL and OpenMP are near the roofline and are essentially BW bound
- OpenACC, and SYCL implementations are still seeing some form of compute bound behavior

<table>
<thead>
<tr>
<th></th>
<th>CUDA</th>
<th>OpenMP*</th>
<th>OpenACC</th>
<th>OpenCL</th>
<th>SYCL*</th>
<th>hipSYCL*</th>
<th>DPCPP*</th>
</tr>
</thead>
<tbody>
<tr>
<td># threads/SM</td>
<td>128</td>
<td>144</td>
<td>N/A</td>
<td>128</td>
<td>144</td>
<td>144</td>
<td>144</td>
</tr>
<tr>
<td>GFLOPS/sec</td>
<td>1111</td>
<td>1028</td>
<td>810</td>
<td>1095</td>
<td>816</td>
<td>767</td>
<td>880</td>
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<td>1269</td>
</tr>
</tbody>
</table>

* result with workaround
## Performance vs. Threads/Workgroup

<table>
<thead>
<tr>
<th># of threads/SM</th>
<th>CUDA</th>
<th>OpenMP*</th>
<th>OpenACC</th>
<th>OpenCL</th>
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<th>hipSYCL*</th>
<th>DPCPP*</th>
</tr>
</thead>
<tbody>
<tr>
<td>36</td>
<td>521.9</td>
<td>757.1</td>
<td>810.0</td>
<td>599.4</td>
<td>498.6</td>
<td>466.7</td>
<td>520.3</td>
</tr>
<tr>
<td>64</td>
<td>1025.1</td>
<td>985.3</td>
<td>1056.7</td>
<td>780.6</td>
<td>741.4</td>
<td>878.1</td>
<td></td>
</tr>
<tr>
<td>72</td>
<td>1103.2</td>
<td>921.2</td>
<td>1083.7</td>
<td>774.1</td>
<td>758.2</td>
<td>879.3</td>
<td></td>
</tr>
<tr>
<td>128</td>
<td>1111.5</td>
<td>1005.5</td>
<td>1095.2</td>
<td>786.6</td>
<td>742.8</td>
<td>870.8</td>
<td></td>
</tr>
<tr>
<td>256</td>
<td>1108.0</td>
<td>1020.5</td>
<td>1092.4</td>
<td>806.1</td>
<td>756.8</td>
<td>872.0</td>
<td></td>
</tr>
</tbody>
</table>

**su3_bench: Performance vs. Threads/SM**

- CUDA & OpenCL
  - Require at least 64 threads/block
  - Near roofline performance
- OpenMP, OpenACC, & SYCL
  - Still seem to have computational inefficiencies
# Measured Roofline (using nvprof)

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<th>DPCPP*</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLOPs</td>
<td>1.00</td>
<td>0.92</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
<td>0.92</td>
<td>0.92</td>
<td>1.00</td>
<td>0.92</td>
</tr>
<tr>
<td>DRAM read</td>
<td>1.11</td>
<td>1.30</td>
<td>1.17</td>
<td>1.12</td>
<td>1.11</td>
<td>41.09</td>
<td>1.11</td>
<td>1.11</td>
<td>1.11</td>
</tr>
<tr>
<td>DRAM write</td>
<td>1.11</td>
<td>4.07</td>
<td>1.12</td>
<td>1.44</td>
<td>1.09</td>
<td>243.89</td>
<td>1.48</td>
<td>1.47</td>
<td>1.48</td>
</tr>
<tr>
<td>measured Roofline</td>
<td>1144</td>
<td>473</td>
<td>1108</td>
<td>992</td>
<td>1152</td>
<td>9</td>
<td>978</td>
<td>985</td>
<td>978</td>
</tr>
</tbody>
</table>

- Pre-workaround, OpenMP and SYCL implementations were moving a lot of data!
  - SYCL still has high write ratio
- DRAM read ratio of 1.11 is ideal
  - Actual AI is 1.35 including other elements in the site structure, 1.5 / 1.35 = 1.11
- FLOP counts depend on the compiler
  - C += A * B; for 3x1 vectors
  - 1.00 – All ops are FMA
  - 0.92 – 1st accumulation of 3x1 vector-vector multiply is an assignment
Performance vs. Measured Roofline

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<td>992</td>
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<td>978</td>
<td>985</td>
<td>978</td>
</tr>
</tbody>
</table>

• CUDA, OpenMP and OpenCL are near the roofline and are essentially BW bound
• OpenACC, and SYCL implementations are moving more data and have a lower roofline, in particular writes
Results for AMD Vega 20: OLCF Lyra test bed

- HIP and OpenCL perform well, but not as good as CUDA on Nvidia’s Volta
  - Same 4 stacks of HBM as Volta
  - hipSYCL limitation?
Results for Intel Gen9/NEO: ALCF Iris test bed

<table>
<thead>
<tr>
<th></th>
<th>OpenCL</th>
<th>DPCPP</th>
<th>OpenMP</th>
</tr>
</thead>
<tbody>
<tr>
<td># threads/SM</td>
<td>36</td>
<td>36</td>
<td>36</td>
</tr>
<tr>
<td>GFLOPS/sec</td>
<td>34.6</td>
<td>34.5</td>
<td>33.4</td>
</tr>
<tr>
<td>roofline</td>
<td>38.4</td>
<td>38.4</td>
<td>38.4</td>
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</table>

su3_bench

**Performance vs. Threads/Block**

- OpenCL
- DPCPP
- OpenMP*

GFLOPS/second vs. threads/block
Programming Model vs. Architecture

<table>
<thead>
<tr>
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<th>SYCL</th>
<th>DPCPP</th>
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<tbody>
<tr>
<td>Nvidia</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X(1)</td>
<td>X(2)</td>
</tr>
<tr>
<td>AMD</td>
<td>X</td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td>X(3)</td>
<td></td>
</tr>
<tr>
<td>Intel</td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

1. ComputeCPP with POCL, which is experimental/unsupported; ComputeCPP also supports a NVPTX backend, but it’s deemed experimental and had performance issues with su3_bench
2. This study used DPCPP as a SYCL compiler, SYCL extensions are untested
3. hipSYCL only at this point in time; ComputeCpp doesn’t support GCN backend, perhaps POCL works?
Performance Portability

<table>
<thead>
<tr>
<th>Programming Model Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cori GPU</td>
</tr>
<tr>
<td>Lyra</td>
</tr>
<tr>
<td>Iris</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cross Platform Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>OpenMP</td>
</tr>
<tr>
<td>OpenCL</td>
</tr>
<tr>
<td>SYCL</td>
</tr>
</tbody>
</table>

Getting good OpenMP performance can be a challenge

- **Su3_bench** includes four (4) different OpenMP implementations
  - All 4 seem to be reasonable solutions
  - Drastically varied performance
  - Still necessary to tune with `num_teams()` and `thread_limit()` directives

- We have explored Clang, Cray CCE, NVIDIA/PGI and Intel compilers and runtimes
  - Using su3_bench to explore OpenMP compilers and runtimes is a presentation in itself!

**Clang release-10.x results**

Version 0: Nominal version (see OpenMP issue slide)
Version 1: Manually distribute sites across teams
Version 2: Work item version (see OpenMP issue slide)
Version 3: Uses collapse(4) over outer loop
Summary and conclusions

• Su3_bench is an open benchmark developed to explore exascale era languages, compilers and runtimes
  • https://gitlab.com/NERSC/nersc-proxies/su3_bench
• Roofline analysis shows that the benchmark is memory bound, however it is more than just another STREAM benchmark
  • A non-trivial complex matrix-matrix multiply kernel with multiple loop nests
  • Initial analysis discovered serious compiler issues that significantly limited performance
  • Even after workarounds and optimizations, performance varies up to 30% across the different programming environments
• Analysis has been performed across NVIDIA, AMD and Intel GPUs
  • Performance portability is good across architectures
  • All languages can target the NVIDIA GPU, not a surprising conclusion given its longevity in the market
• There has been extensive use of su3_bench in evaluating OpenMP compilers and runtimes, results of which are beyond the time allowed by this venue
  • However, if you’re interested we’d be happy to work with you
Future Work

• Need to incorporate more realistic memory access patterns
  • Although the SU(3) multiplications represent LQCD codes, the lattice site access patterns of su3_bench do not
  • Higher level Dslash stencil operation proxy-application is desirable

• Need to incorporate Lattice QCD methods that allow effective use of SIMD for CPU targets?
  • Typically incorporates a data reordering technique to allow adjacent sites to have better spatial locality and hence better utilization of long SIMD lengths